METHOD OF MANUFACTURING ELEMENT CHIP

BACKGROUND

1. Technical Field

The present disclosure relates to a method of manufacturing element chips by dividing a substrate having multiple element regions for each element region.

2. Description of the Related Art

An element chip such as a semiconductor element is manufactured by individually dividing a substrate of a wafer shape having multiple element regions (refer to, for example, PTL 1). In the related art disclosed in PTL 1, a back surface of a wafer is first ground in a state where a front surface of the wafer on which a circuit is formed is attached to a dicing tape, and furthermore, the wafer is thinned by etching. Thereafter, masking is performed by forming a resist layer on a region corresponding to the element regions, and plasma etching is performed, and thereby the wafer is divided into individual semiconductor elements.

Citation List

Patent Literature

PTL 1: JP-A-2002-93752

SUMMARY

As described above, an individual element chip diced from a substrate of a wafer shape is packaged, thereby being used as a device, and in addition to this, there is a case where the element chip such as a flip chip is moved to an electronic component mounting process as it is. In this case, the element chip is mounted in a manner in which a circuit-formed surface directly comes into contact with a conductive material such as a solder paste or a silver paste for bonding. There is a case where the conductive material pushed and widened when the element chip is mounted is wet and spreads to not only a bonding portion of the circuit-formed surface but also a side surface or a back surface of the element chip, that is, so-called “crawling-up” occurs, during the mounting process. The crawling-up of the conductive material causes a short-circuit to occur between electrodes adjacent to each other or an unnecessary electric circuit to be formed on a side surface of the element chip, and thus, various abnormalities such as an increase of current consumption occurs. Therefore, it is necessary to prevent the crawling-up of the conductive material during the mounting process from occurring.

Hence, an object of the present disclosure is to provide a method of manufacturing element chips by which crawling-up of a conductive material is prevented from occurring during a mounting process.

A method of manufacturing element chips according to the present disclosure is a method of manufacturing element chips in which multiple element chips are formed by dividing a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface by using the division region, and includes the following configuration. That is, the method includes preparing the substrate on which an etching resistant layer is formed such that the first surface side is supported by a carrier, a region of the second surface facing the element regions is covered, and a region of the second surface facing the division region is exposed; and performing plasma processing on the substrate which is supported by the carrier after the preparing. The performing of the plasma processing includes dividing and forming of a protection film. In the dividing, the substrate is divided into element chips by etching regions of the substrate which are not covered with the etching resistant layer, in a depth direction of the substrate until reaching the first surface after the second surface is exposed to first plasma, and the element chips having first surfaces, second surfaces, and side surfaces connecting the first surfaces to the second surfaces, are held with an interval between the element chips on the carrier. In the forming of the protection film, the protection film is formed on the side surfaces of the element chips by exposing the element chips to second plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the dividing, and a raw material gas of the second plasma is a mixed gas of fluorocarbon and helium.

A method of manufacturing element chips according to the present disclosure is a method of manufacturing element chips in which multiple element chips are formed by dividing a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface by using the division region, and includes the following processes. That is, the method includes preparing the substrate on which an etching resistant layer is formed such that the second surface side is supported by a carrier, the element regions are covered, and the division region is exposed; and performing plasma processing on the substrate which is supported by the carrier after the preparing. The performing of the plasma processing includes dividing and forming of a protection film. In the dividing, the substrate is divided into element chips by etching regions of the substrate which are not covered with the etching resistant layer, in a depth direction of the substrate until reaching the second surface after the first surface is exposed to first plasma, and the element chips having first surfaces, second surfaces, and side surfaces connecting the first surfaces to the second surfaces, are held with an interval between the element chips on the carrier. In the forming of the protection film, the protection film is formed on the side surfaces of the element chips by exposing the element chips to second plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the dividing, and a raw material gas of the second plasma is a mixed gas of fluorocarbon and helium.

According to the present disclosure, it is possible to prevent crawling-up of a conductive material during a mounting process from occurring.

DESCRIPTION OF DRAWINGS

FIG. 1A is a process explanatory view of a first example illustrating a method of manufacturing element chips according to an exemplary embodiment of the present disclosure;

FIG. 1B is a process explanatory view of the first example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 1C is a process explanatory view of the first example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 2A is a process explanatory view of the first example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 2B is a process explanatory view of the first example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 2C is a process explanatory view of the first example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 3 is a configuration explanatory diagram of a plasma etching apparatus used for the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 4A is a configuration explanatory diagram of the element chip manufactured by the first example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 4B is a configuration explanatory diagram of the element chip manufactured by the first example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 4C is a configuration explanatory diagram of the element chip manufactured by the first example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 4D is a configuration explanatory diagram of the element chip manufactured by the first example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 5A is a process explanatory view of a second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 5B is a process explanatory view of the second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 5C is a process explanatory view of the second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 6A is a process explanatory view of the second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 6B is a process explanatory view of the second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 6C is a process explanatory view of the second example illustrating the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 7A is a configuration explanatory diagram of the element chip manufactured by the second example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 7B is a configuration explanatory diagram of the element chip manufactured by the second example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure;

FIG. 7C is a configuration explanatory diagram of the element chip manufactured by the second example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure; and

FIG. 7D is a configuration explanatory diagram of the element chip manufactured by the second example of the method of manufacturing the element chips according to the exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Next, an exemplary embodiment of the present disclosure will be described with reference to the accompanying drawings. To begin with, a first example of a method of manufacturing element chips according to the present exemplary embodiment will be described with reference to FIG. 1A to FIG. 4D. According to the method of manufacturing the element chips illustrated in the figures, a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface is divided by the division region to form multiple element chips.

As illustrated in FIG. 1A, substrate 1 has a wafer shape in which multiple element chips 10 (refer to FIG. 1C) have element portions 2. Multiple element regions 2a partitioned by division region 1c are formed on first surface 1a that is an element surface on which element portions 2 are formed, in substrate 1. Substrate 1 is moved to a preparation process for manufacturing the element chips, and is supported by carrier 4 and then a mask is formed, as will be described below. A member which can be handled by fixing substrate 1 that is thin and is easily bent, such as an adhesive sheet or a supporting substrate, is used as carrier 4.

In the preparation process, the first surface 1a side of substrate 1 is supported by holding surface 4a of carrier 4, and etching resistant layer 3 is formed by a resist mask, a surface protection layer, or the like which functions as a mask in plasma dicing on second surface 1b, as illustrated in FIG. 1B. That is, etching resistant layer 3 is formed on second surface 1b such that a region of second surface 1b facing element region 2a is covered and region 1d of second surface 1b facing division region 1c is exposed.

After the preparation process is performed by doing so, carrier 4 is moved to a plasma processing process such that plasma processing is performed on substrate 1 supported by carrier 4. A configuration of plasma etching apparatus 20 used in the plasma processing process will be described with reference to FIG. 3. In FIG. 3, the inside of chamber 21 which is a vacuum container is processing room 21a for performing plasma processing, and stage 22 on which carrier 4 supporting substrate 1 which is a processing target is mounted is disposed on the bottom of processing room 21a. Antenna 23 functioning as an upper electrode is disposed on an upper surface of the top of chamber 21, and antenna 23 is electrically connected to first high-frequency power supplier 24. Stage 22 in processing room 21a functions as a lower electrode for plasma processing, and stage 22 is electrically connected to second high-frequency power supplier 25.

Chamber 21 is connected to vacuum exhaust portion 27 through outlet 21c, and processing room 21a enters a vacuum state by driving vacuum exhaust portion 27. Furthermore processing room 21a is connected to plasma generating gas supplier 26 for generating plasma through gas inlet 21b. Plasma etching apparatus 20 described in the present exemplary embodiment can selectively supply multiple types of a plasma generating gas according to an object of plasma processing. Here, first gas 26a, second gas 26b, third gas 26c, or etching gas 26d can be selected as the plasma generating gas.

A gas having an excellent effect with respect to silicon used as a target, such as SF6 or C4F8, is used as first gas 26a. In the present exemplary embodiment, first gas 26a is used for generating first plasma P1 dividing substrate 1 by using plasma etching. A mixed gas of fluorocarbon and helium, such as C4F8, C2F6, CF4, C6F6, C6F4H2, CHF3, or CH2F2 is used as second gas 26b. The gases are used as a plasma CVD gas forming a membrane by using plasma processing, and in the present exemplary embodiment, the gases are used for the purpose of forming a protection film on side surfaces of element chips 10 obtained by dividing substrate 1. A ratio between a total amount of flow of the mixed gas and the amount of flow of helium is appropriately set according to a combination of various gases. It is recommended that the ratio between the total amount of flow of the mixed gas and the amount of flow of helium is 10% to 80% as an illustrative value.

A gas having an excellent physical etching effect, such as oxygen gas or argon gas, is used as third gas 26c. In the present exemplary embodiment, third gas 26c is used for the purpose of sputtering in which an unnecessary portion of the aforementioned protection film is removed. In addition, etching gas 26d is oxygen gas, and is used for the purpose of removing a resin film such as etching resistant layer 3 after a mask function is performed, in the present exemplary embodiment.

During plasma processing performed by plasma etching apparatus 20, substrate 1 which is a processing target is first mounted on stage 22 together with carrier 4, and processing room 21a enters a vacuum state by driving vacuum exhaust portion 27. Together with this, the plasma generating gas according to the purpose of plasma processing is supplied into processing room 21a by plasma generating gas supplier 26 and is maintained at a predetermined pressure. In this state, high-frequency power is supplied to antenna 23 by first high-frequency power supplier 24, and thereby plasma is generated in chamber 21a in accordance with a type of the supplied plasma generating gas. At this time, a bias voltage is applied to stage 22 which is a lower electrode by second high-frequency power supplier 25, and thereby a bias operation can be performed to promote moving of the plasma generated in processing room 21a toward stage 22, and anisotropic etching can be performed by an increased plasma processing effect in a desired specific direction.

In the plasma processing process, processing performed by first plasma P1 is first performed by using first gas 26a. As illustrated in FIG. 1C, second surface 1b of substrate 1 is exposed to first plasma P1, and thereby region 1d (refer to FIG. 1B) of substrate 1 which is not covered with etching resistant layer 3 is etched in a depth direction of substrate 1 (refer to arrows e) until reaching first surface 1a. Accordingly, etching grooves 11 (refer to FIG. 2A) separating respective element chips 10 are formed, and substrate 1 is divided into diced element chips 10. That is, in a state of substrate 1, element chips 10, each having first surface 10a which is first surface 1a, second surface 10b which is second surface 1b, and side surface 10c connecting first surface 10a to second surface 10b, are in a state of being held with an interval between the element chips on carrier 4 (division process).

In the division process, etching conditions can be appropriately selected in accordance with a material of substrate 1. In a case where substrate 1 is a silicon substrate, a so-called Bosch process can be used for etching of the division process. In the Bosch process, a deposition film depositing step, a deposition film etching step, and a silicon etching step are sequentially repeated, and thereby region 1d which is not covered with etching resistant layer 3 can be vertically burrowed in a depth direction of the substrate.

For example, conditions of the deposition film depositing step may be set such that a pressure of processing room 21a is adjusted to 15 to 25 Pa while C4F8 is supplied in 150 to 250 sccm as a raw material gas, power of 1500 to 2500 W is applied to antenna 23 from first high-frequency power supplier 24, power of 0 W is applied to the lower electrode from second high-frequency power supplier 25, and a processing time is 5 to 15 sec. For example, conditions of the deposition film etching step may be set such that the pressure of processing room 21a is adjusted to 5 to 15 Pa while SF6 is supplied in 200 to 400 sccm as a raw material gas, power of 1500 to 2500 W is applied to antenna 23 from first high-frequency power supplier 24, power of 100 to 300 W is applied to the lower electrode from second high-frequency power supplier 25, and a processing time is 2 to 10 sec. Here, sccm is a unit indicating the amount of flow of a gas. That is, 1 sccm indicates the amount of flow of a gas that flows by 1 cm3 per minute at 0°C and 1 atmosphere (standard condition).

For example, conditions of the silicon etching step may be set such that the pressure of processing room 21a is adjusted to 5 to 15 Pa while SF6 is supplied in 200 to 400 sccm as a raw material gas, power of 1500 to 2500 W is applied to antenna 23 from first high-frequency power supplier 24, power of 50 to 200 W is applied to the lower electrode from second high-frequency power supplier 25, and a processing time is 10 to 20 sec. Under the conditions, the deposition film depositing step, the deposition film etching step, and the silicon etching step are repeated, and thereby the silicon substrate can be burrowed at a speed of 10 mm/min.

Thereafter, etching is performed to remove etching resistant layer 3 in a state of covering second surface 10b, in diced element chip 10. That is, as illustrated in FIG. 2A, etching plasma is generated in processing room 21a by using etching gas 26d in plasma etching apparatus 20, and thereby etching resistant layer 3 which uses a resin as main components is removed by etching. Hence, second surface 10b of diced element chip 10 is in a state of being exposed.

Etching conditions can be appropriately selected in accordance with a material of etching resistant layer 3. For example, in a case where etching resistant layer 3 is a resist film, the pressure of processing room 21a may be adjusted to 5 to 15 Pa while oxygen is supplied in 150 to 250 sccm and CF4 is supplied in 0 to 50 sccm as raw material gases, power of 1500 to 2500 W may be applied to antenna 23 from first high-frequency power supplier 24, and power of 0 to 30 W may be applied to the lower electrode from second high-frequency power supplier 25. Under the conditions, etching resistant layer 3 can be removed at a speed of approximately 1 mm/min.

Subsequently, a protection film forming process is performed after the aforementioned division process. That is, second plasma P2 is generated by using second gas 26b which is a mixed gas of fluorocarbon and helium, in processing room 21a of plasma etching apparatus 20, and thereby, element chips 10 are exposed to second plasma P2 in a state of being held with an interval between the element chips on carrier 4, as illustrated in FIG. 2B. Accordingly, protection films 12b and 12c are respectively formed on second surface 10b and side surface 10c of element chip 10.

The protection films are formed for the purpose of preventing a conductive material from crawling up during a mounting process in which element chip 10 is directly bonded to a package substrate or the like, and thus, it is preferable that hygroscopicity is reduced and composition is dense. In the present exemplary embodiment, a mixed gas of fluorocarbon and helium is used as a raw material gas of second plasma P2 used for forming the protection films, and thus, a fluorocarbon film containing fluorine and carbon can be formed as the protection film, and a protection film with decreased hygrocopicity, dense composition, and excellent adhesiveness can be formed. In the protection film forming process, a high-frequency bias is applied to stage 22 (refer to FIG. 3) on which carrier 4 is mounted. Accordingly, injection of ions into element chip 10 is promoted, and thus, it is possible to form a protection film which is denser and has increased adhesiveness.

For example, conditions of forming the protection film may be set such that the pressure of processing room 21a is adjusted to 15 to 25 Pa while C4F8 is supplied in 150 sccm and He is supplied in 50 sccm as raw material gases, power of 1500 to 2500 W is applied to antenna 23 from first high-frequency power supplier 24, and power of 50 to 150 W is applied to the lower electrode from second high-frequency power supplier 25. Under the conditions, processing is performed for 300 sec, and thereby a protection film with a thickness of 3 mm can be formed.

In the present exemplary embodiment, the mixed gas of fluorocarbon and helium is used as a raw material gas. In this way, by mixing helium, divergence of a raw material gas is promoted in the plasma, and as a result, it is possible to form a protection film which is dense and has increased adhesiveness.

In the aforementioned condition example, a ratio between the total amount of flow of the raw material gas and the amount of flow of He is 25% (= 50 / (150 + 50) ´ 100). It is preferable that the ratio is between 10% and 80%, as will be described below. That is, if the ratio between the total amount of flow of the raw material gas and the amount of flow of He is greater than 10%, divergence of the raw material gas is easily promoted in the plasma, and as a result, the protection film which is denser and has increased adhesiveness is easily formed. Meanwhile, if the ratio between the total amount of flow of the raw material gas and the amount of flow of He is greater than 80%, a ratio of C4F8 to the raw material gas is reduced, and thus, supplying of components (C, F, and compound thereof) in the plasma contributing to formation of the protection film into a surface of the substrate is insufficient, a speed of depositing the protection film on the surface of the substrate is delayed, and productivity is reduced.

Subsequently, a protection film removing process is performed in which an unnecessary portion of the protection film formed in the protection film forming process is removed. In the aforementioned protection film forming process, protection film 12b is also formed on side surface 10c of element chip 10 and second surface 10b (refer to FIG. 2B). Since protection film 12b is unnecessary, mask processing for removing the protection film is performed by using third plasma P3.

That is, third plasma P3 is generated by using third gas 26c containing argon gas or oxygen gas as components in processing room 21a of plasma etching apparatus 20, and element chips 10 are exposed to third plasma P3 in a state of being held with an interval between the element chips on carrier 4, as illustrated in FIG. 2C. Thereby, protection film 12c formed on side surface 10c of element chip 10 remains, and protection film 12b formed on second surface 10b exposed on the upper surface of element chip 10 is removed by an etching operation of third plasma P3. Accordingly, second surfaces 10b of element chips 10 held with an interval between the element chips on carrier 4 are in a state of being exposed, and protection film 12e attached to an upper surface of carrier 4 is also removed.

In the aforementioned protection film removing process, a high-frequency bias is applied to the stage on which carrier 4 is mounted. Thereby, it is possible to increase anisotropy of the etching operation of third plasma P3. Hence, protection film 12b of second surface 10b exposed on the upper surface can be reliably removed, and protection film 12c can remain by preventing the etching operation from being performed for protection film 12c of side surface 10c of element chip 10.

For example, conditions of removing the protection film may be set such that the pressure of processing room 21a is adjusted to 0.2 to 1.5 Pa while Ar is supplied in 150 to 250 sccm and O2 is supplied in 0 to 150 sccm as raw material gases, power of 1500 to 2500 W is applied to antenna 23 from first high-frequency power supplier 24, and power of 150 to 300 W is applied to the lower electrode from second high-frequency power supplier 25. Under the conditions, the protection film exposed on the upper surface can be etched at a speed of approximately 0.5 mm/min.

FIGS. 4A to 4D illustrate variation of element chip 10 manufactured by the aforementioned manufacturing process. Element chip 10A illustrated in FIG. 4A shows element chip 10 passing through the protection film forming process illustrated in FIG. 2B, and not only protection film 12c formed on side surface 10c but also protection film 12b formed on second surface 10b remain. Element chip 10B illustrated in FIG. 4B shows element chip 10 passing through the protection film removing process illustrated in FIG. 2B, and protection film 12b is removed from second surface 10b. At this time, an upper end portion of protection film 12c formed on side surface 10c becomes removal portion 12cx whose outer edge portion is partially removed by the etching operation of the third plasma.

In addition, in element chip 10C illustrated in FIG. 4C, a range is expanded in which an upper end portion of protection film 12c formed on side surface 10c is removed, and exposure portion 10e in which an upper end portion of side surface 10c is exposed is formed. Furthermore, in element chip 10D illustrated in FIG. 4D, the upper end portion of side surface 10c is removed by etching an end portion of exposure portion 10e which is exposed, and thereby corner-cut portion 10ex is formed.

All element chips 10A to 10D are configured to include first surface 10a having element region 2a in which element portion 2 is formed, second surface 10b on a side opposite to first surface 10a, and side surface 10c connecting first surface 10a to second surface 10b. In element chips 10A to 10D having the aforementioned configurations, protection film 12c with surface properties preventing a conductive adhesive material from wetting and spreading is formed in a range in which the conductive adhesive material comes into contact with at least side surface 10c during a mounting process, and thus, it is possible to prevent the conductive material from crawling up during the mounting process. In addition, since element chip 10D includes corner-cut portion 10ex, a bending strength of the element chip can increase.

Next, a second example of a method of manufacturing the element chips according to the present exemplary embodiment will be described with reference to FIGS. 5A to 5C, FIGS. 6A to 6C, and FIGS. 7A to 7D. Here, according to the method of manufacturing the element chips described in the second example, a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface is divided by the division region to form multiple element chips, in the same manner as in the first example.

As illustrated in FIG. 5A, substrate 1 has a wafer shape in which multiple element chips 10 (refer to FIG. 5A) have element portions 2. Multiple element regions 2a partitioned by division region 1c are formed on first surface 1a that is an element surface on which element portions 2 are formed, in substrate 1. Substrate 1 is moved to a preparation process for manufacturing the element chips, and is supported by carrier 4 and then a mask is formed, as will be described below. A member which can be handled by fixing substrate 1 that is thin and is easily bent, such as an adhesive sheet or a supporting substrate, is used as carrier 4, in the same manner as in the first example 1.

In the preparation process, second surface 1b side of substrate 1 is supported by holding surface 4a of carrier 4, and etching resistant layer 3 functioning as a mask is formed on first surface 1a by plasma dicing, as illustrated in FIG. 5B. That is, etching resistant layer 3 is formed on first surface 1a such that element region 2a is covered and division region 1c is exposed.

After the preparation process is performed as described above, carrier 4 is moved to a plasma processing process such that plasma processing is performed on substrate 1 supported by carrier 4. Plasma etching apparatus 20 (refer to FIG. 3) described in the first example is used in the plasma processing process.

In the plasma processing process, processing performed by first plasma P1 is first performed by using first gas 26a. As illustrated in FIG. 5C, first surface 1a of substrate 1 is exposed to first plasma P1, and thereby region 1c (refer to FIG. 5B) of substrate 1 which is not covered with etching resistant layer 3 is etched in a depth direction of substrate 1 (refer to arrows e) until reaching second surface 1b. Accordingly, etching grooves 11 (refer to FIG. 6A) separating respective element chips 10 are formed, and substrate 1 is divided into diced element chips 10. That is, in a state of substrate 1, element chips 10, each having first surface 10a which is first surface 1a, second surface 10b which is second surface 1b, and side surface 10c connecting first surface 10a to second surface 10b, are in a state of being held with an interval between the element chips on carrier 4 (division process).

Thereafter, etching is performed to remove etching resistant layer 3 in a state of covering second surface 10b, in diced element chip 10. That is, as illustrated in FIG. 6A, etching plasma is generated in processing room 21a by using etching gas 26d in plasma etching apparatus 20, and thereby etching resistant layer 3 which uses a resin as a main component is removed by etching. Hence, second surface 10b of diced element chip 10 is in a state of being exposed.

Subsequently, a protection film forming process is performed after the aforementioned division process. That is, second plasma P2 is generated by using second gas 26b which is a mixed gas of fluorocarbon and helium, in processing room 21a of plasma etching apparatus 20, and thereby, element chips 10 are exposed to second plasma P2 in a state of being held with an interval between the element chips on carrier 4, as illustrated in FIG. 6B. Accordingly, protection films 12a and 12c are respectively formed on first surface 10a and side surface 10c of element chip 10.

Advantages and effects of using the mixed gas of fluorocarbon and helium as a raw material gas of second plasma P2 during forming of the protection film are the same as those of the first example. In addition, a high-frequency bias is applied to a stage on which carrier 4 is mounted during the protection film forming process. Accordingly, injection of ions into element chip 10 is promoted, and thus, it is possible to form a protection film which is denser and has increased adhesiveness.

Subsequently, a protection film removing process is performed in which an unnecessary portion of the protection film formed in the protection film forming process is removed. In the aforementioned protection film forming process, protection film 12a is also formed on side surface 10c of element chip 10 and first surface 10a (refer to FIG. 6B). Since protection film 12a is unnecessary, mask processing for removing the protection film is performed by using third plasma P3.

That is, third plasma P3 is generated by using third gas 26c containing argon gas or oxygen gas as components in processing room 21a of plasma etching apparatus 20, and element chips 10 are exposed to third plasma P3 in a state of being held with an interval between the element chips on carrier 4, as illustrated in FIG. 6C. Thereby, protection film 12c formed on side surface 10c of element chip 10 remains, and protection film 12a formed on first surface 10a exposed on the upper surface of element chip 10 is removed by an etching operation of third plasma P3. Accordingly, first surfaces 10a of element chips 10 held with an interval between the element chips on carrier 4 are in a state of being exposed, and protection film 12e attached to an upper surface of carrier 4 is also removed.

In the aforementioned protection film removing process, a high-frequency bias is applied to the stage on which carrier 4 is mounted. Thus, it is possible to increase anisotropy of the etching operation of third plasma P3. Hence, protection film 12a of first surface 10a exposed on the upper surface can be reliably removed, and protection film 12c can remain by preventing the etching operation from being performed for protection film 12c of side surface 10c of element chip 10.

FIGS. 7A to 7D illustrate variation of element chip 10 manufactured by the aforementioned manufacturing process. Element chip 10A illustrated in FIG. 7A shows element chip 10 passing through the protection film forming process illustrated in FIG. 5B, and not only protection film 12c formed on side surface 10c but also protection film 12a formed on first surface 10a remain. Element chip 10B illustrated in FIG. 7B shows element chip 10 passing through the protection film removing process illustrated in FIG. 5B, and protection film 12a is removed from first surface 10a. At this time, an upper end portion of protection film 12c formed on side surface 10c becomes removal portion 12cx whose outer edge portion is partially removed by the etching operation of the third plasma.

In addition, in element chip 10C illustrated in FIG. 7C, a range is expanded in which an upper end portion of protection film 12c formed on side surface 10c is removed, and exposure portion 2c is formed in which a side end portion of element portion 2 formed on an upper end portion of first surface 10a is exposed. Furthermore, in element chip 10D illustrated in FIG. 7D, an end portion of exposure portion 2c is removed by etching, and thereby corner-cut portion 2cx is formed.

All element chips 10A to 10D are configured to include first surface 10a having the element region in which element portion 2 is formed, second surface 10b on a side opposite to first surface 10a, and side surface 10c connecting first surface 10a to second surface 10b. In element chips 10A to 10D having the aforementioned configurations, protection film 12c is formed in a range in which the conductive adhesive material comes into contact with at least side surface 10c during a mounting process, and thus, it is possible to prevent the conductive material from crawling up during the mounting process and the same effects as those of the first example are obtained. In addition, since element chip 10D includes corner-cut portion 2cx, a bending strength of the element chip can increase.

A method of manufacturing element chips according to the present disclosure obtains effects in which a conductive material can be prevented from crawling up during a mounting process, and is effective in a field in which the element chips are separated by dividing a substrate including multiple element regions for each element region.

WHAT IS CLAIMED IS:

1. A method of manufacturing element chips in which multiple element chips are formed by dividing a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface by using the division region, the method comprising**:**

preparing the substrate on which an etching resistant layer is formed such that the first surface side is supported by a carrier, a region of the second surface facing the element regions is covered, and a region of the second surface facing the division region is exposed; and

performing plasma processing on the substrate which is supported by the carrier after the preparing,

wherein the performing of the plasma processing includes,

dividing the substrate into element chips by etching regions of the substrate which are not covered with the etching resistant layer, in a depth direction of the substrate until reaching the first surface after the second surface is exposed to first plasma to hold the element chips having first surfaces, second surfaces, and side surfaces connecting the first surfaces to the second surfaces, with an interval between the element chips on the carrier, and

forming a protection film on the side surfaces of the element chips by exposing the element chips to second plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the dividing, and

wherein a raw material gas of the second plasma is a mixed gas of fluorocarbon and helium.

2. The method of manufacturing element chips of Claim 1, wherein a high-frequency bias is applied to a stage on which the carrier is mounted during the forming of the protection film.

3. The method of manufacturing element chips of Claim 1, further comprising:

forming the protection film on the second surfaces together with the side surfaces of the element chips during the forming of the protection film; and

removing the protection film formed on the second surfaces of the element chips by making the protection film formed on the side surfaces of the element chips remain, by exposing the element chips to third plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the forming of the protection film.

4. The method of manufacturing element chips of Claim 3, wherein a high-frequency bias is applied to a stage on which the carrier is mounted during the removing of the protection film.

5. A method of manufacturing element chips in which multiple element chips are formed by dividing a substrate including a first surface having multiple element regions partitioned by a division region and a second surface on a side opposite to the first surface by using the division region, the method comprising**:**

preparing the substrate on which an etching resistant layer is formed such that the second surface side is supported by a carrier, the element regions are covered, and the division region is exposed; and

performing plasma processing on the substrate which is supported by the carrier after the preparing,

wherein the performing of the plasma processing includes,

dividing the substrate into element chips by etching regions of the substrate which are not covered with the etching resistant layer, in a depth direction of the substrate until reaching the second surface after the first surface is exposed to first plasma to hold the element chips having first surfaces, second surfaces, and side surfaces connecting the first surfaces to the second surfaces, with an interval between the element chips on the carrier, and

forming a protection film on the side surfaces of the element chips by exposing the element chips to second plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the dividing, and

wherein a raw material gas of the second plasma is a mixed gas of fluorocarbon and helium.

6. The method of manufacturing element chips of Claim 5, wherein a high-frequency bias is applied to a stage on which the carrier is mounted during the forming of the protection film.

7. The method of manufacturing element chips of Claim 5, further comprising:

forming the protection film on the first surfaces together with the side surfaces of the element chips during the forming of the protection film; and

removing the protection film formed on the first surfaces of the element chips by making the protection film formed on the side surfaces of the element chips remain, by exposing the element chips to third plasma in a state where the element chips are held with an interval between the element chips on the carrier, after the forming of the protection film.

8. The method of manufacturing element chips of Claim 7, wherein a high-frequency bias is applied to a stage on which the carrier is mounted during the removing of the protection film.

ABSTRACT OF THE DISCLOSURE

In a plasma processing process used for a method of manufacturing element chips by which multiple element chips are manufactured by dividing a substrate having multiple element regions, the substrate is exposed to first plasma, and thereby the substrate is divided into element chips, and the element chips having first surfaces, second surfaces, and side surfaces connecting the first surfaces to the second surfaces are held with an interval between the element chips on the carrier. The element chips are exposed to second plasma which uses a mixed gas of fluorocarbon and helium as a raw material gas, and thereby a protection film covering the side surfaces is formed, and a conductive material is prevented from crawling up to the side surfaces during a mounting process.